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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,614	10/14/2003	Chi-Shun Weng	REAP0011USA	2613

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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
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MERRIFIELD, VA 22116

EXAMINER	
WAMBACH, MARGARET R	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 06/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,614	WENG, CHI-SHUN	
	Examiner	Art Unit	
	Margaret R Wambach	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *1-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *101403*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: The pages of the specification are not numbered. Also, it appears as if Figure 5 illustrates a second example of a second Gray code count sequence, contrary to the Brief Description of the drawing, for instance, consistent with the procedure adopted by applicant in Figure 2.

Appropriate correction is required.

Claim Objections

Claims 1-15 are objected to because of the following informalities: Throughout the claim language, there are instances wherein spaces have not been left between words. For example, in claim 1, "1A" and "abit". Please also note that in every instance, a space was not left between the period after the claim number and the first word of the claim. Furthermore, it appears as if the terms "number" and "element" are used in the claim language to reference the same thing. This creates confusion. In claims 5 and 9, a comma should be inserted before "respectively". In claims 8 and 12, "element" and in claim 15, "input of the AND gate" should be in its plural form. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The disclosure does not clearly teach how to determine a first bit switch sequence, a bit switching sequence property, a second bit switch sequence and a second Gray code count sequence as recited in claim 1. Without such information, one skilled in the art, could not make and use the claimed invention.

In particular, applicant gives two examples of Gray code count sequences and lists steps in Figure 2 which are discussed in the specification but the discussion of these steps and the examples do not provide sufficient detail to permit an understanding of the process recited in claim 1. In fact, the only step which does not require guesswork to interpret is step 10 (which is recited in claim 1) wherein the number of digits for the first gray code count sequence is determined. No further explanation is required for step 10. However, how applicant determines what these digits shall be (step 12 which is also recited in claim 1) is never explained sufficiently in the disclosure. What is the bit switching sequence property referenced in claim 1? There are many, many existing gray codes so if applicant wishes to utilize a prior art gray code for step 12, he should identify the same (applicant appears to reference it as a conventional gray code sequence in paragraph 25 and it appears to be the same full-length gray code disclosed in Yi.) On the other hand, if it is a new gray code, then the manner in which such a pattern is generated should be disclosed. Similarly, how a second bit

switching sequence is determined is described in such vague terms, applicant's intended meaning cannot be deciphered. For example, applicant states that elements are deleted from the first gray code count sequence until the number of elements equals N -1 but the problem is that applicant doesn't clearly explain how one skilled in the art decides which elements should be deleted and the examples don't reveal what methodology is employed. The examiner conjectures that the deletions are made from the pattern based primarily on complying with the "bit sequence property." Unfortunately, the specification never defines what "bit sequence property" means. It is assumed to mean that the code must still remain in gray code after the deletions of elements are made. Thus, in the example of Figure 3, deletion of the element "2" is not allowed because it would break the code. It is also unclear whether there is a difference between the second Gray code sequence and the second bit switch sequence.

With regard to claim 2, although the specification does reference a symmetrical property of the first bit switch sequence and the examiner would guess that the ordered subsets referenced in claim 2 are the mirror image patterns, the specification does not explain how the subsets are formed in language which would allowed one skilled in the art to make and/or use the invention. Further, even if deletions are made symmetrically (with the same digit positions changing), some symmetrical pairs are deleted and some are not. How are the ones that are deleted selected? Does it not matter as long as the code isn't broken? Also, with respect to the different methodology for deleting an odd number rather than an even number, how is the one deletion which doesn't belong to a symmetric pair chosen?

The specification and drawings do not enable the embodiments recited in claims 6 and 10 wherein the values of deleted elements are the same. If the ordinary meaning of "value" is assumed, that would mean that gray code digits of the same value are deleted. Rather, it appears as if gray code digits which are symmetrically arranged around a middle digit are deleted. Similarly, claims 7 and 11 are not enabled because even the examples given by applicant don't show elements in the same positions being deleted. Rather, symmetrical elements having the same digit position changing are deleted in the examples.

The limitations of claims 8 and 12 are not explained by the specification and the drawings such that applicant's intended meaning can be understood. In fact, the examiner is unable to conjecture in these instances applicant's intended meaning.

Allowable Subject Matter

Claims 2-13 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim 1 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Claims 14 and 15 contain allowable subject matter.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yi is very relevant to claim 1; however, referring to Figure 3 and

column 4 of Yi, the first bit switch sequence does not have 2 to the mth power – 1 elements and the second bit switch sequence does not have N-1 elements.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Margaret R Wambach whose telephone number is (571)272- 1756. The examiner can normally be reached on Monday, Tuesday, Thursday and Friday 6am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Margaret R Wambach
Primary Examiner
Art Unit 2816

mrw